WHAT IS CLAIMED IS:

1. A PLL frequency synthesizer for driving a charge pump using an output from a phase comparator for comparing a phase of a frequency of a generation voltage of a voltage-controlled oscillator with a phase of a reference frequency, and driving the voltage-controlled oscillator using an output from the charge pump, thereby outputting a signal having a set desired frequency, characterized in that

when an output voltage and an output current of the charge pump come close to driving limits, a power supply voltage of the voltage-controlled oscillator is changed to cancel a change in input voltage of the voltage-controlled oscillator.

2. A PLL frequency synthesizer for driving a charge pump using an output from a phase comparator for comparing a phase of a frequency of a generation voltage of a voltage-controlled oscillator with a phase of a reference frequency, and driving the voltage-controlled oscillator using an output from the charge pump, thereby outputting a signal having a set desired frequency, characterized in that

a power supply voltage of the voltage-controlled oscillator is controlled based on the set frequency, thereby widening an apparent lock range.

3. A PLL frequency synthesizer for driving a charge

pump using an output from a phase comparator for comparing a phase of a frequency obtained by dividing a frequency of a generation voltage of a voltage-controlled oscillator by a first predetermined frequency division number with a phase of a frequency obtained by dividing a reference frequency by a second predetermined frequency, and driving the voltage-controlled oscillator using an output from the charge pump, thereby outputting a signal having a set desired frequency, characterized by comprising:

a VCO power supply voltage setting device for setting a power supply voltage of the voltage-controlled oscillator, and a controller for controlling a set voltage of the VCO power supply voltage setting device on the basis of the set frequency.

4. A PLL frequency synthesizer according to claim 3, further comprising a buffer amplifier for protecting the voltage-controlled oscillator from an abrupt variation at a load portion of the PLL frequency synthesizer.

5. A PLL frequency synthesizer according to claim 3, wherein said controller sets the first and second predetermined frequency division numbers to set a frequency of a signal output from the PLL frequency synthesizer.

6. A radio communication apparatus characterized by comprising said PLL frequency synthesizer defined in any one of claim 1.

7. A radio communication apparatus characterized by comprising said PLL frequency synthesizer defined in any one of claim 2.

8. A radio communication apparatus characterized by comprising said PLL frequency synthesizer defined in any one of claim 3.

9. A radio communication apparatus characterized by comprising said PLL frequency synthesizer defined in any one of claim 4.

10. A radio communication apparatus characterized by comprising said PLL frequency synthesizer defined in any one of claim 5.

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